[Abstract] [PDF Full-Text (395 KB)] **IEEE CNF**

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Device Research Conference, 2003 , 23-25 June 2003
Pages:39 - 40

[Abstract] [PDF Full-Text (290 KB)] **IEEE CNF**

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VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on , 10-12 June 2003
Pages:119 - 120

[Abstract] [PDF Full-Text (261 KB)] **IEEE CNF**

Very Low Defects and High Performance Ge-On-Insulator p-MOSFETs with Al_2O_3 Gate Dielectrics

C. H. Huang[1], M. Y. Yang[1], Albert Chin[1], W. J. Chen[2], C. X. Zhu[3], B. J. Cho[3], M.-F. Li[3], and D. L. Kwong[4]

[1]Dept. of Electronics Eng., National Chiao Tung Univ., Hsinchu, Taiwan
[2]Dept. of Mechanical Materials Eng., National Yun-Lin Polytechnic Inst., Huwei, Taiwan
[3]Si Nano Device Lab., Dept. of Electrical & Computer Eng., National Univ. of Singapore, Singapore
[4]Dept. of Electrical & Computer Engineering, The Univ. of Texas, Austin, TX 78712, USA

Abstract

We demonstrate for the first time high quality and dislocation free Ge-on-insulator (GOI) p-MOSFETs with Al_2O_3 gate dielectrics [EOT=1.7nm]. Compared to control Al_2O_3/Si p-MOSFETs, the Al_2O_3/GOI devices show similar leakage current for the same EOT, 2X increase in drive current, and 2.5X increase in hole mobility. In addition, the Al_2O_3/GOI devices exhibit 1.3X enhanced hole mobility over the SiO_2/Si universal hole mobility at E_{eff} of 1MV/cm.

Introduction

Pure Ge channel MOSFETs have attracted much attention due to its enhanced electron and hole mobility over conventional Si-MOSFET [1]. These improvements are especially important for high-κ gate dielectric MOSFETs where the mobility degradation is the main technology bottleneck. Both strained and relaxed Ge channel and Ge bulk p-MOSFETs have recently been reported [2]-[3]. In this paper, we demonstrate for the first time high quality and dislocation free Ge-on-insulator (GOI) p-MOSFETs with Al_2O_3 gate dielectrics [4]. This low defects are mandatory for real VLSI manufacture (<1 dislocation/cm^2) to achieve a high yield. In additional to the orders of magnitude lower defect density than strained Si or relaxed SiGe on Si, the Al_2O_3/GOI devices show similar leakage current for the same EOT, 2X increase in drive current, and 2.5X increase in hole mobility compared to control Al_2O_3/Si p-MOSFETs. In addition, the Al_2O_3/GOI devices exhibit 1.3X enhancement of hole mobility over the SiO_2/Si universal mobility.

Experimental

After depositing 75 nm SiO_2 on Ge and Si wafers, the GOI was formed by bonding SiO_2/Ge and SiO_2/Si at 500°C for 10 hrs. To enhance the bonding at such low temperature, O_2 plasma was used to activate the SiO_2 surface before bonding [5] and a constant pressure was applied during bonding process. After etch back, a 400nm isolation SiO_2 was deposited on Ge. The p$^+$ source and drain were formed by implanting B^+, followed by 500°C furnace anneal. Al_2O_3 gate dielectric [4] was deposited on Ge, followed by Al gate electrode formation. For comparison, $Al_2O_3/Si_{0.3}Ge_{0.7}$ and Al_2O_3/Si p-MOSFETs were also fabricated, where a solid-phase epitaxy was used to form the $Si_{0.3}Ge_{0.7}$ on Si [3].

Results and Discussion

A. GOI characterization

Fig. 1 shows the X TEM of GOI wafer. The different contrast between top and bottom layers is due to the different electron scattering of Ge and Si atoms and small crystal orientation misalignment. No defect can be observed on top Ge. To our knowledge, this is the first demonstration of defect free GOI structure. The GOI structure was further characterized by Energy Dispersive Spectroscopy (EDS) shown in Fig. 2, and a Ge layer on SiO_2/Si was confirmed. An interfacial layer at the bonding interface and middle of SiO_2 is due to the O_2 plasma treatment [5]. Very smooth Ge/SiO_2 interface, comparable SOI, is achieved, and is essential for ultra-thin body GOI MOSFET.

B. Al_2O_3/GOI capacitor and reliability

Figs. 3 and 4 present the respective J-V and C-V characteristics of Al_2O_3 capacitors on GOI, $Si_{0.3}Ge_{0.7}$/Si, and Si substrates. Comparable leakage current is observed for these devices with similar EOT=1.7nm from C-V measurement. A $Jg=1.5\times10^{-3}$ A/cm^2 at 1V for Al_2O_3/GOI with EOT=1.7nm is 3 orders of magnitude lower than that in SiO_2/Si. Good reliability for Al_2O_3/GOI gate dielectric is evidenced from the high t_{BD} and MTTF, as shown in Fig. 5, and is comparable to Al_2O_3/Si devices. An extrapolated max operating voltage of 2.5V is obtained for 10 years lifetime.

C. Al_2O_3/GOI p-MOSFET and mobility

Figs. 6 and 7 show the I_d-V_d of $Al_2O_3/Si_{0.3}Ge_{0.7}$/Si and Al_2O_3/GOI, respectively, and the control Al_2O_3/Si device is also shown in Fig. 6. Significant enhancement in I_d for both Al_2O_3/GOI and $Al_2O_3/Si_{0.3}Ge_{0.7}$/Si over Al_2O_3/Si devices is observed, with the Al_2O_3/GOI device showing the highest I_d. The relatively large $I_{d\text{-}OFF}$ shown in Fig. 8 can be improved by thinning down the top Ge layer. The effective mobility is plotted in Fig. 9. As can be seen clearly, the hole mobility increases with increasing Ge content, where the mobility for $Al_2O_3/Si_{0.3}Ge_{0.7}$/Si and Al_2O_3/GOI are 1.7X and 2.5X, respectively, higher than Al_2O_3/Si control device at E_{eff} of 1.0MV/cm. The hole mobility is also 1.3X higher than the published universal mobility data from thermal SiO_2/Si at 1MV/cm E_{eff}.

Conclusions

We have demonstrated for the first time a defect free GOI structure and a high performance Ge p-MOSFET with Al_2O_3 gate dielectric (EOT=1.7nm). Results show that Al_2O_3/GOI p-MOSFET has low gate leakage current of 1.5×10^{-3} A/cm^2 at 1V and 2.5X enhancement in hole mobility over control Al_2O_3/Si devices. In addition, the Al_2O_3/GOI devices exhibit 1.3X enhancement of hole mobility over the SiO_2/Si universal mobility at E_{eff} of 1MV/cm.

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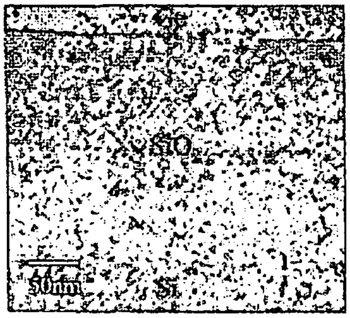

Fig. 1. Cross-sectional TEM of GOI. The different contrast between the top Ge and bottom Si substrate is due the different atomic scattering of electron beams and small crystal orientation misalignment. No dislocations can be observed in GOI.

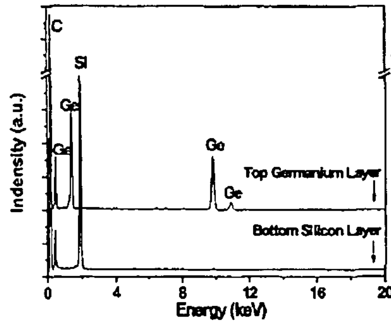

Fig. 2. The measured Energy Dispersive Spectroscopy from top and bottom layers, which confirms the GOI structure shown in Fig. 1. The Carbon signal is from the glue.

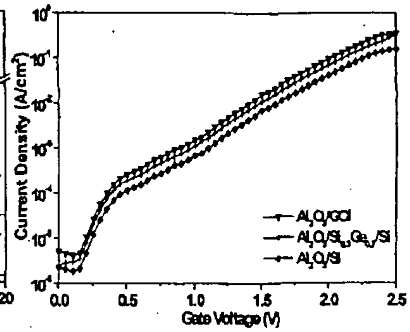

Fig. 3. The measured J-V characteristics of Al_2O_3 gate dielectric on GOI, $Si_{0.3}Ge_{0.7}/Si$ and Si. The comparable gate leakage current indicates that high quality Al_2O_3 gate dielectric can be formed on GOI.

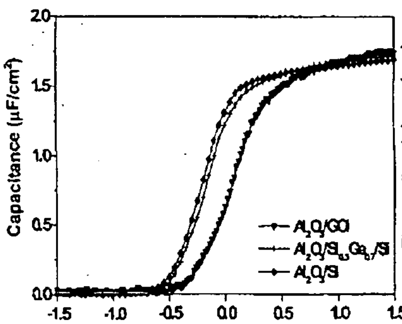

Fig. 4. The 1MHz C-V characteristics of Al_2O_3 gate dielectric on GOI, $Si_{0.3}Ge_{0.7}/Si$ and Si. A k value of 9 and EOT of 1.7nm are obtained.

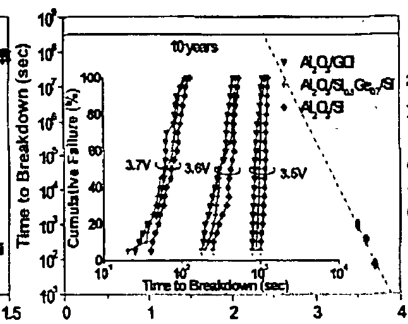

Fig. 5. The measured and extrapolated Mean-Time to Failure MTTF as a function of gate voltage from the inserted dielectric breakdown time t_{BD} distribution plot.

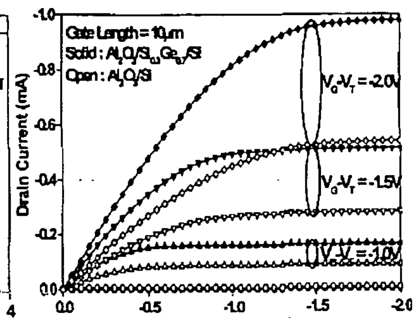

Fig. 6. The I_d-V_d characteristics of $Al_2O_3/Si_{0.3}Ge_{0.7}/Si$ and Al_2O_3/Si p-MOSFETs. At the same V_g-V_t, the I_d from $Al_2O_3/Si_{0.3}Ge_{0.7}/Si$ device is 1.8X higher than Al_2O_3/Si control p-MOSFETs.

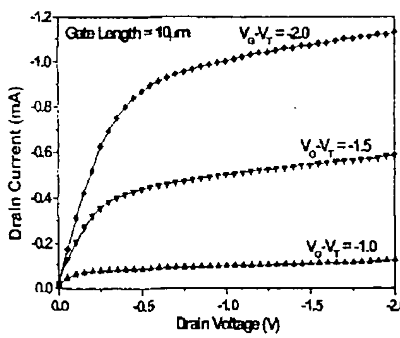

Fig. 7. The I_d-V_d characteristics of Al_2O_3/GOI PMOSFETs. At the same V_g-V_t, the I_d from Al_2O_3/GOI device is 2.0X higher than Al_2O_3/Si control p-MOSFETs in Fig. 6.

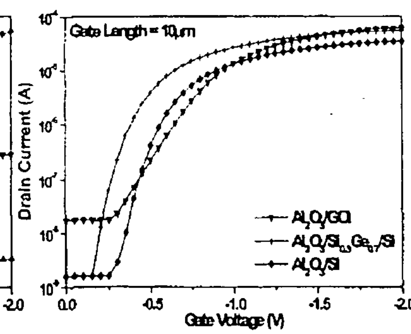

Fig. 8. The I_d-V_g characteristics of Al_2O_3/GOI, $Al_2O_3/Si_{0.3}Ge_{0.7}/Si$ and Al_2O_3/Si p-MOSFETs. At the same 10μm gate length, the I_d from Al_2O_3/GOI device is the highest than others that is due to the highest Ge%.

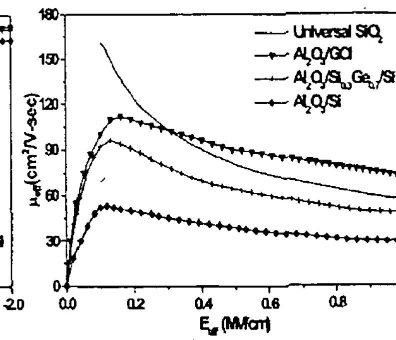

Fig. 9. The hole mobility of Al_2O_3/GOI, $Al_2O_3/Si_{0.3}Ge_{0.7}/Si$ and Al_2O_3/Si p-MOSFETs. The hole mobility increases with increasing Ge content and is higher than the universal SiO_2/Si hole mobility at GOI device.